The MSM3000™ dual-mode CDMA + AMPS ASIC:
for increased functionality and standby time of handsets
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Abstract — The MSM3000 dual mode ASIC for digital baseband processing within CDMA Cellular[1] handsets is a significant leap forward in functionality. The improvements include an upgraded microprocessor, several standby time improvements, an upgraded vocoder DSP to allow for cost effective EVRC, and support for multiple code channel reception for packet data service speeds up to 86.4 kbps in the forward direction per new TIA standards.

I Introduction
The MSM3000 is the fifth generation integrated Mobile Station Modem™ (MSM) produced by QUALCOMM, Incorporated[2]. Its predecessor, the MSM2300™, was an achievement in cost savings, reduced idle current, and CDMA searcher speed. The MSM3000 builds upon this successful architecture, and additionally incorporates:

- A 32-bit RISC microprocessor
- Higher rate data capability per IS-95-B
- Increased standby time
- EVRC support in the vocoder DSP

The MSM3000 is a digital baseband ASIC that enables manufacturers to meet or exceed the specifications of mobile stations for cdmaOne systems worldwide, including IS-95-A/B and its variants in PCS, South America, Korea, and Japan. This paper will briefly summarize these features with emphasis on improved standby time.

II ASIC Statistics
The MSM3000 ASIC, made in a CMOS process, operates at $V_{dd} = 2.7 - 3.6$ Volts. It is available in several packaging options, including a 196-ball PBGA (15mm x 15mm) and a 176-ball FBGA (13mm x 13mm).

See Figure 1 for a high-level diagram of interfaces.

The chip design was completed in January 1998, sampled in July, and entered volume production in December, including system software and reference phone design.

<table>
<thead>
<tr>
<th>Mode at $V_{dd}=2.8$ V</th>
<th>Typical</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{dd}$</td>
<td>0.070</td>
<td>0.225</td>
</tr>
<tr>
<td>CDMA slotted paging</td>
<td>20*</td>
<td>27*</td>
</tr>
<tr>
<td>awake and receiving</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CDMA Rx/Tx EVRC</td>
<td>47*</td>
<td>62*</td>
</tr>
</tbody>
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*Add about 5mA to run microprocessor from 27 MHz

III RISC Microprocessor
The previous generations of QUALCOMM MSMs integrated the Intel 80186 microprocessor. While sufficient in its day and rich in support, the 80186 suffers from several drawbacks compared with modern microprocessor cores.

The ARM7TDMI from ARM® supports 32-bit ARM7 & 16-bit thumb mode instructions. The advantages of the ARM7TDMI include:

- 4 gigabytes of addressable memory space
- Higher performance at same clock rate due to RISC architecture with 3 stage pipelining.
- Code density; ARM is estimated to need 30% less code than 80186.
- Power savings, it is completely static.
- Silicon area and cost savings, it is about 40% smaller than the 80186.

The MSM3000 supports both a full in-circuit emulator (ICE) and a reduced pin-out JTAG in-phone debugging solution. The chip also includes a Serial Bus Interface (SBI) master controller, a 3-pin serial interface to the internal registers of the IFR3000, IFT3000, and other external devices for low bandwidth control.

IV Higher Data Rate
The CDMA Standard IS-95-B[3] defines supplemental traffic channels for optional support of higher speed CDMA data services. Additionally, the IS-707-A standard defines a packet data service option and a new radio link protocol that works on top of the faster traffic channels. Prior to these standards’ development the maximum available raw data of CDMA data was 14,400 kbps.
bps. The new higher data rates may be configured asymmetrically between the downstream (forward) and upstream (reverse) directions.

With a goal of providing greater than 64 kbps in the forward link, the MSM3000 design achieves:
- Up to 8 channels of 9,600 bps (76.8 kbps), or
- Up to 6 channels of 14,400 bps (86.4 kbps).

The increased data traffic impacts the design in several areas. Additional parallel integrator circuits are added to three of the RAKE "Finger" despreader circuits. The fourth finger only works in single channel mode, as the MIPS to process four fingers in high speed mode were not available. In consideration of available MIPS, the demodulator DSP clock optionally switches to a higher clock frequency to achieve the MIPS needed for 3 finger HDR. The deinterleaver's frame and decoder's output buffers were increased in size to support the higher number of bits per 20 ms frame. Also, the decoder architecture was enhanced to achieve higher throughput.

Finally, the instruction cycles available to the microprocessor, which must handle each byte of data, are of concern. Loading tests with 16-bit wide external SRAM on the memory bus show promising results running HDR with the internal ARM. (Of course, the internal bus-sizer also supports 8-bit SRAM for lower phone cost without HDR.)

V. Increased Standby Time

The CDMA standby time has been increased using several techniques within the MSM3000: the improved microprocessor already described, a VCTCXO shutdown feature, a faster Viterbi Decoder, several reset features, and highly optimized software control algorithms. Much of the complexity in software is to tightly control the timing of hardware events in slotted mode, and to efficiently manage the searching for idle handoff candidates.

V.A VCTCXO Shutdown

Thus far, the Qualcomm MSM product line has been tailored to phones that are built around a single frequency reference for the modem functions, a 19.68 MHz voltage-controlled, temperature-compensated, crystal oscillator (VCTCXO). This reference was the only one in the phone of sufficient quality to accurately run the sleep counter that instructed the phone when to wake up and monitor slots on the CDMA paging channel. The start of each slot occurs every 2.56 or 5.12 seconds in practice, and the time reference related timing errors are desired to be kept to ±10 microsecond range. This would dictate that the sleep counter frequency be known to within ±2 ppm. To achieve this error, previous designs have run the sleep counter off of the stable and accurate 19.68 MHz VCTCXO. However the VCTCXO and its isolation buffer consume 2 to 3 mA of current. This now impacts standby time significantly.

Uncorrected quartz crystals may have significant frequency variation over temperature, but their sensitivity is fairly low, especially when compared with other low power options. In fact, the tuning fork type quartz crystals that are used commonly in wristwatches are very low power and inexpensive. They typically run at 32.768 kHz and have a frequency to temperature relationship of:

$$\Delta f = -0.04(T - 25)^2,$$

where $\Delta f$ is the fraction frequency error in ppm, and $T$ is the temperature in degrees Celsius. This leads to about 5 ppm/C at the temperature of 85°C. As temperature variation within a phone can be on the order of 2°C/min or more, a technique that closely tracks varying frequency offset dynamically is needed.

Thus, the MSM3000, includes a sleep counter that is partially clocked from a lower power source which allows the VCTCXO to be powered-off. The improved sleep counter works jointly off the long periods of the low power clock for most of the sleep cycle and the finer periods of the VCTCXO clock at the start and end of the sleep cycle. This allows the CDMA modem core to be disabled for an accurate predetermined amount of time. The MSM3000 integrates a frequency calibration circuit, which beats the VCTCXO clock against the low power clock to help initiate the calibration process. Note, that the VCTCXO is corrected during CDMA signal reception to typically better than 0.1 ppm. Also the MSM3000 integrates the inverters necessary to complete the oscillation circuits for crystals in the vicinity of 32 kHz and 2 MHz in frequency.

V.B Decoder Reset

Conventionally, a Viterbi Decoder needs to start decoding a stream several constraint lengths prior to the significant messages in order that their state metrics converge beyond an arbitrary starting state. Since the IS-95[4] paging channel includes a 20 ms frame interleaver, the conventional receiver is forced to begin demodulating and decoding at least 20 ms prior to the start of the slot's first message.

Section 7.7.2.1.2 of IS-95 was modified in making IS-95-B to include a better-defined encoding state at the start of paging slots. This change calls for the paging channel to guarantee padding bits when the start of slot is coincident with the start of a new message. The padding bits are defined to be 4 or more zero bits at the
end of the previous slot. This standards change reduces the throughput of the channel only in a very few configurations of message length, as the half-frame length of 95 bits in 9600 bps paging is not divisible by 8, and all messages must be an integer multiple of 8 bits in length. This change introduces no backward compatibility problems, as the padding was previously optional.

By more fully knowing the transmit encoder’s state at the start of the slot, the receiver may be able to begin the demodulation process 20 ms later, increasing the phone’s battery life. Standby time improvements on the order of 5 to 20% are possible due to this alone.

The 256 state metrics of a K=9 Viterbi decoder represents the running log-likelihood metric for the most likely bit sequence that goes through the particular encoder state of interest. State metric memory is internally maintained as non-negative integers, with the 0 value being the very best possible metric. Thus, upon a decoder reset corresponding to \(n=4\) known zero padding bits, the first \(2^{K-1-n}=16\) state metrics are simply reset to 0, and the remaining 240 states are set to the maximum value.

Simulations are used to verify the performance of this reset scheme, for the rate \(\frac{1}{2}\) encoded 9600 bps paging stream. Figure 2 shows simulation results of Message Error Rate (MER) for the Rayleigh fading channel, with a message length of 300 bits. A loss in performance of about 0.1 dB is measured in a variety of cases, a rather small amount. The MER measures are for the first message of the slot, starting exactly on the slot boundary. This Monte-Carlo symbol-level simulation of each point stops upon collecting 1,000 message errors. Also the pilot channel is taken to be noise-free here for simplicity.

V.C CDMA Standby Time Estimate

Detailed phone-level current estimation predict that phones may achieve a CDMA standby time of 200 hours on a 800 mAh battery using this ASIC.

VII EVRC Vocoder

A new 8 kbps speech compression standard, known as Enhanced Variable Rate Coder (EVRC) was standardized by the TIA in IS-127. To achieve the higher level of voice quality, increased MIPS, program memory, and coefficient memory are needed by the vocoder’s DSP. The Qualcomm Digital Signal Processor (QDSP1) core has been upgraded to the QDSP1+ core in the MSM3000. The core is speed up to run at 20 MHz in the MSM3000, as in the MSM2310™, which also offered EVRC support. The instructions memory has been converted to ROM to save die area. The vocoder also supports 8 kbps QCELP (IS-96), and 13 kbps PureVoice (IS-733) speech compression standards for CDMA.

VIII Conclusion

A brief overview of a complex ASIC for wireless communications has been presented. The focus has been on the improvements beyond its several predecessors, with special focus on standby time and higher speed data.

IX Acknowledgements

The authors would like to thank the entire MSM3000 team. Individually the authors are indebted to Mr. S. Patel for the simulation results presented; and Dr. P. Black and Mr. K. Easton for much of the technical inspiration.

X References


Figure 1 Conceptual diagram of MSM3000 functions integrated in a phone

Rayleigh Fading, MER vs. Eb/No [dB]

Figure 2 Message Error Rate (MER) in a 1-Path Rayleigh Fading Channel